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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,734	07/24/2003	Naoto Fujishima	1639.1008D	8062

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,734	FUJISHIMA, NAOTO	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/156,757.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The non-final rejection as set forth in paper No. (120804) mailed on December 10th, 2004 is withdrawn in response to applicants' amendments. A new rejection is made as set forth in this Office Action. New dependent claim 5 is added to recite feature in an alternate fashion. Thus, claims (1-5) are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

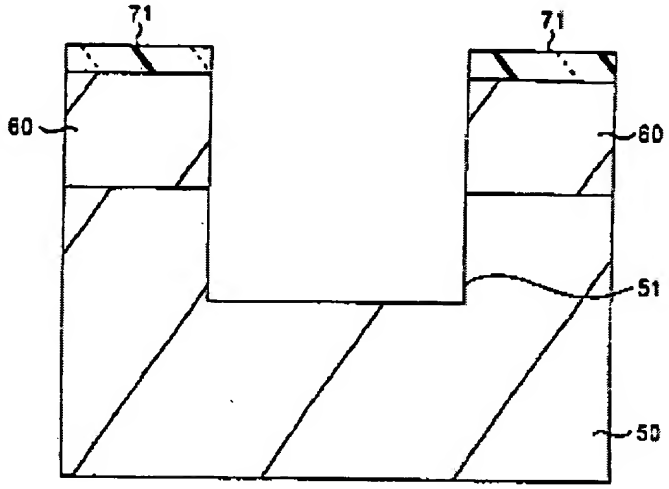
Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujishima et al. (U.S. Patent 6,781,197).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 1, **Fujishima** discloses a method for manufacturing a semiconductor device, comprising:

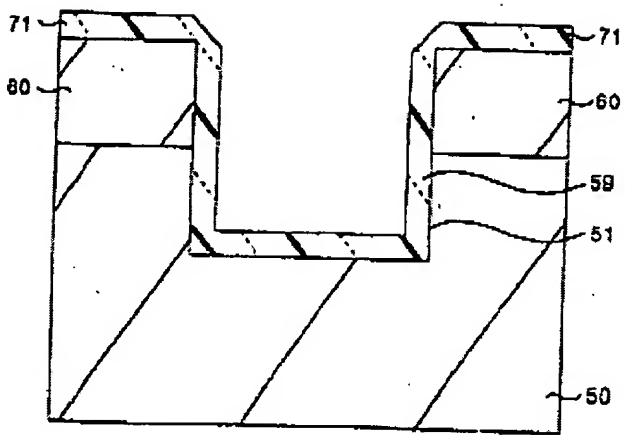
forming a trench **51** in a surface region of a semiconductor substrate **50**, of a first conductivity type (p-type); forming a drift region **60** (n-type), of a second conductivity type, around the trench **51** (col. 6, lines 9-44 and FIG. 5);

Fig. 5



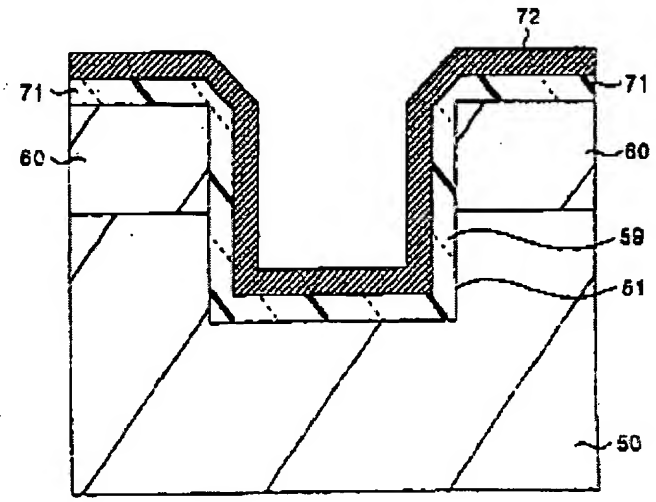
forming a gate insulating film **59**, having a uniform thickness, along a side surface and a bottom surface of the trench **51** and inside the trench **51** (col. 6, lines 45-54 and FIG. 6);

Fig. 6



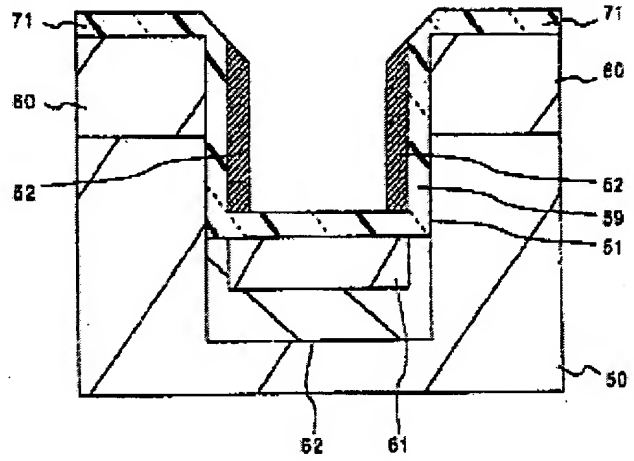
forming a first conductor **72** along a surface of the gate insulating film **59**, etching back the first conductor **72** in an active region so that the first conductor remains only in side surface regions of the trench (col. 6, lines 54-57 and col. 7, lines 3-9 and FIGS. 7 and 10);

Fig. 7



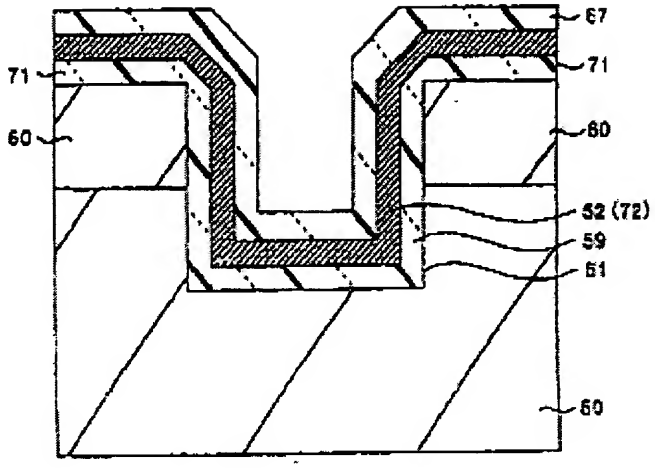
forming a base region (p-type) **62** of, the first conductivity type, and a source region (n-type) **61**, of the second conductivity type, in a surface region of the semiconductor substrate **50** outside the trench **51** (col. 7, lines 10-25 and FIG. 10);

Fig. 10



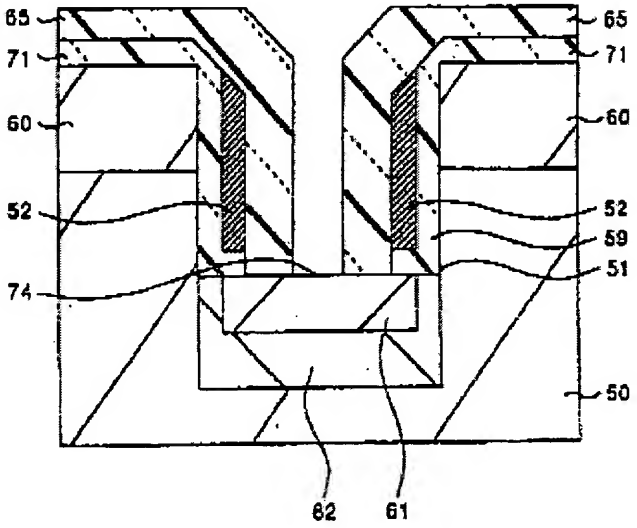
forming an interlayer dielectric **65, 67** inside the first conductor **72** (col. 7, lines 51-61 and FIG. 11);

Fig. 11



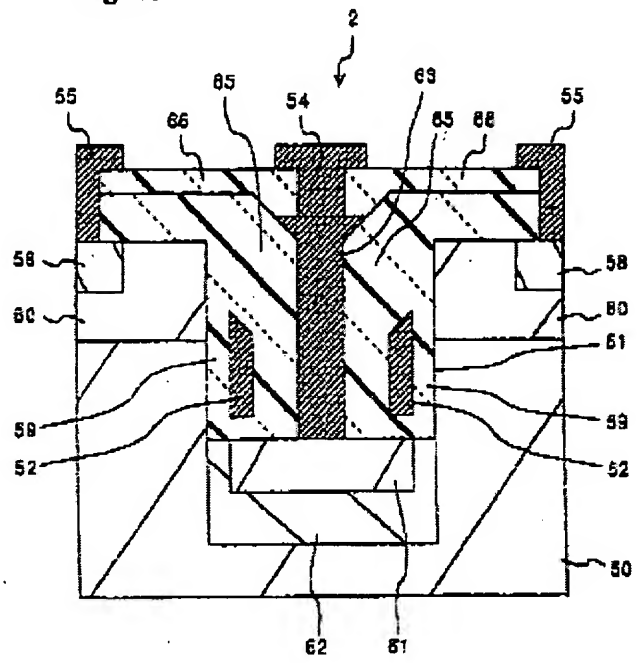
selectively removing a bottom of the interlayer dielectric **65** in the active region (col. 7, lines 51-61 and FIG. 14);

Fig. 14



forming a drain region **61** (n-type) of, the second conductivity type, at the bottom of the trench **51** (col. 7, lines 5-61 and FIG. 16); and

Fig. 16

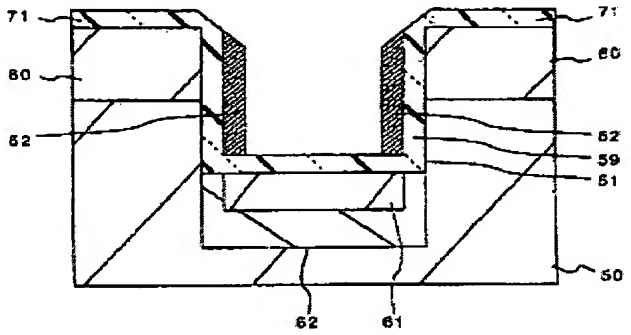


forming a second conductor **63** in the trench **51**, the second conductor **63** electrically connecting to the drain region **61** (col. 7, lines 46-61 and FIG. 16).

In re claim 2, **Fujishima** discloses that the method for manufacturing a semiconductor device of claim 1, further comprising: forming an interlayer dielectric **65**, **67** on a surface of the semiconductor substrate **50**, opening contact holes **74** through the interlayer dielectric; forming a gate electrode **53** that electrically connects to the first conductor **72**, a drain electrode that electrically connects to the second conductor **63**, and a source electrode **54** that electrically connects to the source region **54** (col. 7, lines 38-61 and FIGS. 14-16).

In re claim 3, **Fujishima** discloses that the etching back of the first conductor includes over-etching the first conductor **72** so that only a portion of the first conductor lower than the surface of the semiconductor substrate **50** remains un-removed (FIG. 10).

Fig. 10



In re claim 4, **Fujishima** discloses that etching back the first conductor **72** includes over-etching the first conductor so that only a portion of the first conductor lower than the surface of the semiconductor remains un-removed (FIG. 10).

In re claim 5, **Fujishima** discloses that the trench **51** is formed by one etching (FIG. 5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
June 23rd, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER